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For: VOLTAGE-TO-CURRENT CONVERTER

CLAIM OF PRIORITY AND TRANSMITTAL OF CERTIFIED PRIORITY DOCUMENT

Commissioner for Patents
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Dear Sir:

In accordance with the provisions of 35 U.S.C. 119, Applicant hereby claims, in the present application, the priority of European Patent Application No. 032505744.4, filed February 5, 2003. The certified copy is submitted herewith.

Respectfully submitted,

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Date: February 5, 2004

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The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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R C van Dijk

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Voltage to current converter

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"Voltage-to-current converter"

* * *

The present invention relates to voltage-to-current converters and was developed by paying specific attention to the possible use in circuitry for controlling a laser driver via a microcontroller. However, reference to this application is not to be construed as limiting the scope of the invention.

Microcontroller-supervised systems use digital-to-analog converters (DACs) in order to generate analog voltages used for controlling other devices. While commercial DACs generate a voltage as the analog output, in some cases the device to be controlled is essentially current-driven, which means that the behaviour of the controlled device depends on the current injected into or sunk through its input.

In the case of these current-driven circuits, additional circuitry is required between the DAC and the device controlled. Such additional circuitry is usually in the form of a voltage-to-current converter, which is also currently referred to as a "transconductance" amplifier.

The simplest approach to voltage-to-current conversion is shown in figure 1 and essentially provides for the use of a single, purely passive component such as a resistor.

In the diagram of figure 1, a resistor R is interposed between the output of the DAC and a current-controlled device D, such as a driver unit for a laser source L. The DAC is controlled via a line C by a microcontroller designated M.

If V_{dac} designates the voltage output of the DAC and V_{in} is the voltage at the input of the controlled device D then the current I_{in} input to the device D can be simply expressed as:

$$I_{in}=(V_{dac}-V_{in})/R.$$

This arrangement has the disadvantage that the resulting current I_{in} is not stable when the load voltage

changes. Additionally, there may be an offset in voltage-to-current response that is a zero current for non-zero voltage and/or vice versa.

Also, there is no positive I_{in} for positive V_{dac} if V_{dac} is less than V_{in}. If V_{in} changes (for instance in the presence of a thermal drift in the device to be controlled), I_{in} changes even if the DAC setting (and thus V_{dac}) has not changed, which is undesirable in most applications.

An alternative prior art arrangement is shown in figure 2, where the same references were adopted to designate elements identical or equivalent to those already considered in figure 1.

The arrangement of figure 2 employs an operational amplifier A having a positive (non-inverting) input fed with the output voltage V_{dac} from the DAC and an inverting input fed with the voltage provided by a negative feedback loop comprised of a voltage divider connected between the output of the amplifier A and the ground. The voltage divider in question includes the device D to be controlled and the resistor R.

In this case, if the device D comprising the load of the circuit has an impedance Z_L the current I_{load} flowing through the load can be expressed as:

$I_{load}=V_{dac}/R$.

In this case the load current I_{load} is linear with V_{dac}. However, the load D must be floating, that is both its terminals must be connected to non-ground points. This is seldom true for loads that are active devices such as, for instance, inputs of integrated circuits.

A classic circuit for a ground-terminated load is shown in figure 3.

In this case the voltage V_{dac} is applied to the inverting input of the amplifier A via first resistor B1 while another resistor B4 is connected as a feedback resistor between the amplifier output and the inverting input. The resistors B1 and B4 thus comprise a voltage

extending from the intermediate point towards a respective terminal of the sensing resistor so that the sensing resistor is interposed between the first branches of the first and second feedback loops. These loops also include each a second branch with a second resistor extending from the intermediate point to an input port of the converter circuit. The first and second resistors in the feedback loops have resistance values that are substantially higher than the resistance values of the sensing resistor and the load. The current across the sensing resistor constitutes an output current signal proportional to the input voltage signal applied between the input ports of the second branches of the first and the second feedback loops.

The invention will now be described, by way of non-limiting example only, with reference to the annexed figures of drawing, wherein:

- figures 1 to 3, related with the prior art, where already described previously,
- figure 4 is a block diagram of a first circuit according to the invention,
- figure 5 shows a generalization of the circuit of figure 4, and
- figures 6 and 7 shows the possible application of the invention to laser current control.

Throughout figures 4 to 7 the same references already appearing in figures 1 to 3 where used to designate parts or elements (e.g. a microcontroller, a digital to analog converter, and so on) that were already discussed in the foregoing.

Similarly to the arrangement of figure 3, the arrangement of figure 4 provides for the presence of positive and negative feedback loops including voltage dividers, including four resistors, associated with both inputs of the amplifier A.

The arrangement of figure 4 includes a further resistor Rs associated with the output of the amplifier A. In this specific arrangement, that represents one of the

divider between the amplifier output and the DAC output with an intermediate point connected to the inverting input of the amplifier A. Another voltage divider including two resistors B2 and B3 is similarly associated with the non-inverting input of the amplifier A. Specifically, the resistor R3 is connected between the amplifier output and the non-inverting input while the resistor R2 is interposed between the non-inverting input of the amplifier A and the ground. The load D is connected in parallel with the resistor B2.

The main disadvantage of this arrangement lies in that the overall gain is negative. When V_{dac} is positive, I_{load} is negative which in turn means that in order to have a positive I_{load}, V_{dac} must be negative. This is incompatible with a single supply voltage arrangement, and most current applications use single, positive-only or negative-only, supply voltages, which makes it impossible to use the arrangement shown in figure 3.

The object of the present invention is thus to provide an improved arrangement dispensing with the drawbacks that are inherent in the prior art arrangements discussed in the foregoing.

According to the present invention, such an object is achieved by means of a circuit arrangement having the features set forth in the claims that follow.

A preferred embodiment of the invention is thus a voltage-to-current converter, including a differential amplifier having non-inverting and inverting inputs as well as associated circuitry for applying an input voltage signal to the converter and deriving therefrom an output current signal for a load. A sensing resistor is provided for series connection with the load and first and second feedback loops are associated with the non-inverting and inverting inputs of the differential amplifier respectively. Each feedback loop includes an intermediate point connected to a respective input of the differential amplifier, a first branch including a first resistor

many possible embodiments of the invention, the resistor Rs has a first lead or terminal connected to the output of the amplifier A and a second terminal connected to a first terminal of the load D. The opposite terminal of the load D, that has an impedance Z_L, is connected to the ground. The resistor Rs is thus arranged in series with the load D. The current flowing through the load D is designated I_{load}.

A first one of voltage dividers associated with the inputs of the amplifier A comprises a negative feedback loop including:

- a first (upper) branch with a resistor R1 connected between the inverting input of the amplifier A and the terminal of Rs closer to the output of the amplifier A to sense a voltage Vs2, and
- a second (lower) branch with a resistor R2 connected between the inverting input of the amplifier A and the ground.

The second voltage divider associated with the inputs of the amplifier A comprises a positive feedback loop including:

- a first branch with a resistor R1 connected between the terminal of the resistor Rs more remote from the output of the amplifier A to sense a voltage Vs1 and the non-inverting input of the amplifier, and
- a second branch with a resistor R2 through which the output of voltage from the DAC converter, namely V_{dac}, is applied to the non-inverting input of the amplifier A.

The values of the resistors R1 are selected in such a way that the currents flowing through them are in fact negligible so that the current flowing through the sensing resistor Rs is in fact identical to the current I_{load} flowing through the load D.

Due to the action performed by the two feedback loops comprised of the voltage dividers including the resistors R1 and R2, such a current is in fact proportional to the input voltage V_{dac}.

More specifically, solving the network equations ruling the behaviour of the circuit arrangement of figure 4 (which equations and the respective solving procedure are not reported herein as they fall within the current capability of any technician experience in circuit design) shows that, provided R1 is much larger than Rs, Z_L, (where Z_L denotes the impedance value of the load D) the current flowing through the load D, namely I_{load}, can be expressed as:

$I_{load}=(V_{dac}/Rs).(R1/R2)$

Since the resistors R1 are connected to the two ends of Rs, other components (as better explained in the following) can be connected in series with the output of the operational amplifier A - that is between the output of the operational amplifier A and Rs/R1, but this will in no way change the behaviour and operation of the circuit shown.

The feedback resistors R1 (and indirectly R2, since the ratio R1/R2 sets the gain of the transimpedance amplifier) having a value much higher than the resistance/impedance values of the "sensing" resistor Rs and the load Z_L means that the resistors R1, R2 comprising the feedback loops/voltage dividers primarily sense voltages while the currents flowing through them are in fact negligible. Those of skill in the art will appreciate that while an impedance value Z_L, including both resistive (real) and reactive (imaginary) components, is being referred to for the sake of precision, in most practical applications the load D will be essentially resistive. In any case, a resistance value being much higher than an impedance value simply means that the resistance value is much higher than the modulus of the impedance.

Provided these conditions are met, in the arrangement of figure 4 the output current is proportional to the controlling voltage V_{dac}, to the ratio of the values of the feedback resistors R1, R2 and inversely proportional to the value of the sensing resistor Rs. Also the output current

is independent of the load impedance Z_L, thereby implementing a real transconductance amplifier.

The arrangement shown in figure 4 shows no offset (apart from the operational amplifier input offset) and requires only a single supply voltage. The operational amplifier A must be capable of operating with the inputs at the ground voltage. This is a requirement that is currently met by most "rail-to-rail" input operational amplifiers currently available at low cost.

The gain (transconductance) can be set to desired value by properly choosing R1, R2, Rs.

Because the transconductance depends on R1/R2 and Rs, if any constraint exists on one of these factors (for instance Rs), the other factor can be easily adapted in order to obtain the desired gain.

While identical values have been indicated herein for the resistor values (R1 and R2) in the two feedback loops associated with the amplifier, this only represents a preferred choice dictated primarily by the sake of simplicity. The only requirement for proper operation of the arrangement shown herein is that the voltage divider ratios of the positive feedback loop and the negative feedback loop are the same.

The block diagram of figure 5 shows that the arrangement of figure 4 can be generalized by regarding the input voltage V_{dac}, as a differential input voltage (V_a–V_b) applied to the inputs of the amplifier A via the two resistors R2 comprising the second branches of the feedback loops.

Also, the values Vs1 and Vs2 whose difference, namely (Vs2-Vs1), defines the sensing voltage across the resistor Rs may be obtained as a differential value the can be derived from any point of the circuit, provided the resistor Rs is arranged in series with the load D.

In fact, the values of the resistors R1 being selected in such a way that the currents flowing through them are in fact negligible, the current flowing through the sensing

resistor Rs is in fact identical to the current I_{load} flowing through the load D. Due to the action performed by the two feedback loops comprised of the voltage dividers including the resistors R1 and R2, such a current is in fact proportional to the input voltage V_{dac}.

The differential sensing voltage Vs2-Vs1 sensed across the sensing resistor Rs generates a load current I_{load} proportional to the differential voltage input. This also irrespective of any thermal drift or offset voltage Vterm possibly present on the load.

The block B shown in figure 5 may thus be e.g. an amplifier stage, both in the form of a current amplifier and in the form of a voltage amplifier.

The only requirement for the arrangement shown in figure 5, which permits easy implementation of a closed-loop control, is that when the voltage at the operational amplifier output increases also the differential value Vs2-Vs1 must increase, in order to prevent the circuit from oscillating. More generally, the op-amp stability requirements derived from the data-sheet of the operational amplifier A must be met.

The block diagram of figure 6 shows an example of the application of generalized circuit of figure 5 to precisely setting the current of a laser source L driven by a laser current driver comprising the block B.

In fact, in the arrangement of figure 6, the laser L represents the load proper and the current through the laser L is sourced/sunk by the driver B, which acts as a current-controlled current generator.

The following relationship applies:

$(Vs2\text{-}Vs1)=(R1/R2).V_{dac}$

and the current I_{laser} through the laser L can be expressed as:

$I_{laser}=(Vs2\text{-}Vs1)/Rs=(R1/R2)(V_{dac}/Rs)$ when R1, R2 are much larger than Rs.

Also, it will be appreciated that in the arrangement of figure 6 (and in the arrangement of figure 7 as well)

the locations of Vs1 and Vs2 are somewhat exchanged with respect to the arrangement shown in figure 5. In fact, in the arrangements shown in figures 6 and 7, the laser driver B draws the current from the laser L, and the polarity of the load current is reversed with respect to the arrangements shown in figure 5 and previously.

Finally, figure 7 shows another example of application of the circuit with differential input of figure 6. This is done by referring specifically to certain applications wherein the current I_{laser} flowing through the laser L must be shut down slowly, that is with a controlled decreasing slope in order to avoid any sharp changes in power balance in optical amplifiers.

Optical systems usually require the laser source to be shut down within a time interval that is shorter than the time interval, which could be achieved by gradually decreasing the DAC setting. This is because of the minimum timing requirements of the digital communication between the microcontroller and the DAC. Conversely, fully satisfactory operation can be easily achieved by resorting to the arrangement shown in figure 7 that essentially corresponds to the arrangement shown in figure 6 but for the fact that the terminal of the resistor R2 that is grounded in figure 6 is set to a voltage V_{slope}.

The voltage V_{slope} is kept at zero level (that is at ground level) during normal operation of laser L. When gradual turn off of the laser is to be achieved, V_{slope} is caused gradually to rise and such rising signal is subtracted from V_{dac}, effectively reducing the laser current in a controlled way.

A rising slope voltage V_{slope} can be generated in a known manner, for instance by means of a simple RC network including:

- a capacitor Cs connected between the ground and the input of the resistor R2 intended to be fed with the voltage V_{slope},

- a resistor Rsd connected between the input of the resistor R2 intended to be fed with the voltage V_{slope} and a voltage V_T.

A switch such as an electronic switch SW is connected in parallel to the capacitor Cs to keep it grounded (uncharged) during normal operation on the circuit so that V_{slope} is kept at zero level during normal operation of laser L.

When gradual turn off is required, the switch SW is opened, thus permitting the capacitor to be gradually charged towards V_T through the resistor Rsd. The voltage V_{slope} is thus caused gradually to rise and subtracted from D_{dac}, effectively reducing the laser current in a controlled way.

Of course, without prejudice to the underlying principle of the invention, the details and embodiments may vary, also significantly, with respect to what has been described and shown, by way of example only without departing from the scope of the invention as defined by the annexed claims.

CLAIMS

1. A voltage-to-current converter, including a differential amplifier (A) having non-inverting and inverting inputs as well as associated circuitry (R1, R2, Rs) for applying an input voltage signal (V_{dac}) to the converter and deriving therefrom an output current signal (I_{load}) for a load (D) having a given impedance value (Z_L), wherein said output current signal (I_{load}) is proportional to said input voltage signal (V_{dac}), characterized in that:

- a sensing resistor (Rs) is provided for series connection with said load (D),

- first and second feedback loops are associated with said non-inverting and inverting inputs of said differential amplifier (A), respectively; each said feedback loop including:

  - an intermediate point connected to a respective input of said differential amplifier (A),

  - a first branch including a first resistor (R1) extending from said intermediate point towards a respective terminal of said sensing resistor (Rs), said sensing resistor (Rs) being thus interposed between the first branches of said first and second feedback loops, and

  - a second branch including a second resistor (R2) extending from said intermediate point to an input port of said converter circuit,

wherein said respective first resistors in said first and second feedback loops have resistance values (R1) that are substantially higher than the resistance values of said sensing resistor (Rs) and said load (D) and the current across said sensing resistor (Rs) constitutes said output current signal (I_{load}) proportional to said input voltage signal applied between said input ports of the second branches of said the first and the second feedback loops.

2. The converter of claim 1, characterized in that said input voltage signal (v_{dac}) is applied to the input port of the second branch of said first feedback loop, and

in that the input port of said second branch of said second feedback loop is connected to the ground.

3. The converter of claim 1, characterized in that the input ports of the second branches of said first and second voltage feedback loops represent input ports for said conversion circuit having said input voltages signal (V_{dac}) applied therebetween in a differential arrangement.

4. The converter of any of the previous claims, characterized in that said the first resistors in said first branches of said first and second feedback loops have identical resistance values (R1).

5. The converter of any of the previous claims, characterized in that said first and second feedback loops are comprised of voltage dividers (R1, R2), having respective voltage divider ratios defined by said first resistor (R1) in said first branch and said second resistor (R2) in said second branch, and wherein said respective voltage divider are the same for said first and second feedback loops.

6. The converter of any of the previous claims, characterized in that said first branch in said first feedback loop is connected to the output of said differential amplifier (A).

7. The converter of any of the previous claims, characterized in that that said intermediate point in said first feedback loop is connected to the inverting input of said differential amplifier (A).

8. The converter of any of the previous claims, characterized in that said first branch of said second feedback loop is connected between said sensing resistor (Rs) and said load (D)

9. The converter of any of the previous claims, characterized in that that said intermediate point in said second feedback loop is connected to the non-inverting input of said differential amplifier (A).

10. The converter of any of the previous claims, characterized in that it includes a ramp signal generator

(V_T, Rsd, Cs) for selectively (SW) applying to the input port of one of the second branches of said first and second feedback loop a ramp signal for gradually reducing said output current signal (I_{load}).

11. The circuit of any of the previous claims, characterized in that it has associated a laser source (L).

12. The circuit of claim 11, characterized in that it includes a current drive circuit (B) for said laser source (L) and in that said drive circuit (B) is interposed between the output of said differential amplifier (A) and said sensing resistor (Rs) in series with the laser source (L).

ABSTRACT

A voltage-to-current converter, includes a differential amplifier (A) having non-inverting and inverting inputs as well as associated circuitry for applying an input voltage signal to the converter and deriving therefrom an output current signal for a load (D). A sensing resistor (Rs) is provided for series connection with the load and first and second feedback loops are associated with the non-inverting and inverting inputs of the differential amplifier (A), respectively. Each feedback loop includes an intermediate point connected to a respective input of the differential amplifier, a first branch including a first resistor (R1) extending from the intermediate point towards a respective terminal of the sensing resistor (Rs) so that the sensing resistor is interposed between the first branches of the first and second feedback loops. These loops also include each a second branch with a second resistor (R2) extending from the intermediate point to an input port of the converter circuit. The first and resistors in the feedback loops have resistance values that are substantially higher than the resistance values of the sensing resistor (Rs) and the load (D). The current across the sensing resistor (Rs) constitutes an output current signal proportional to the input voltage signal applied between the input ports of the second branches of the first and the second feedback loops.

(Figure 4)

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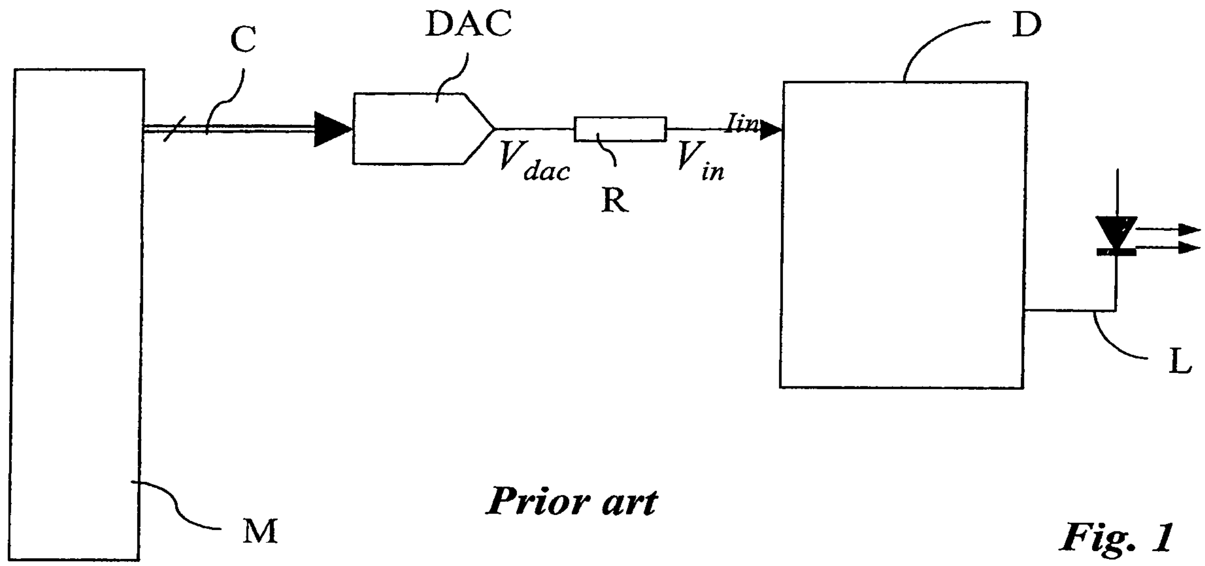
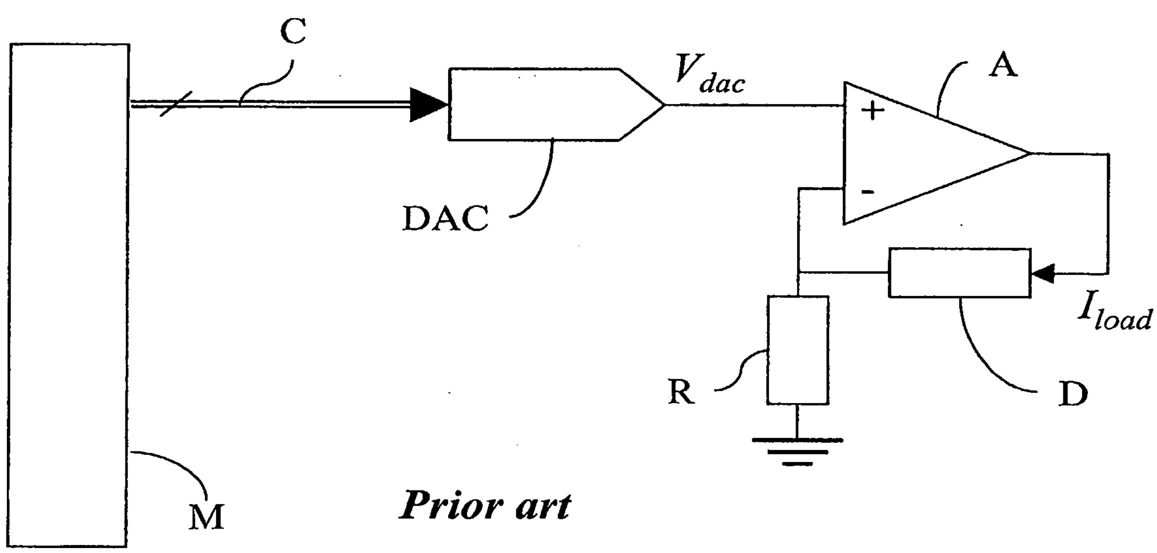


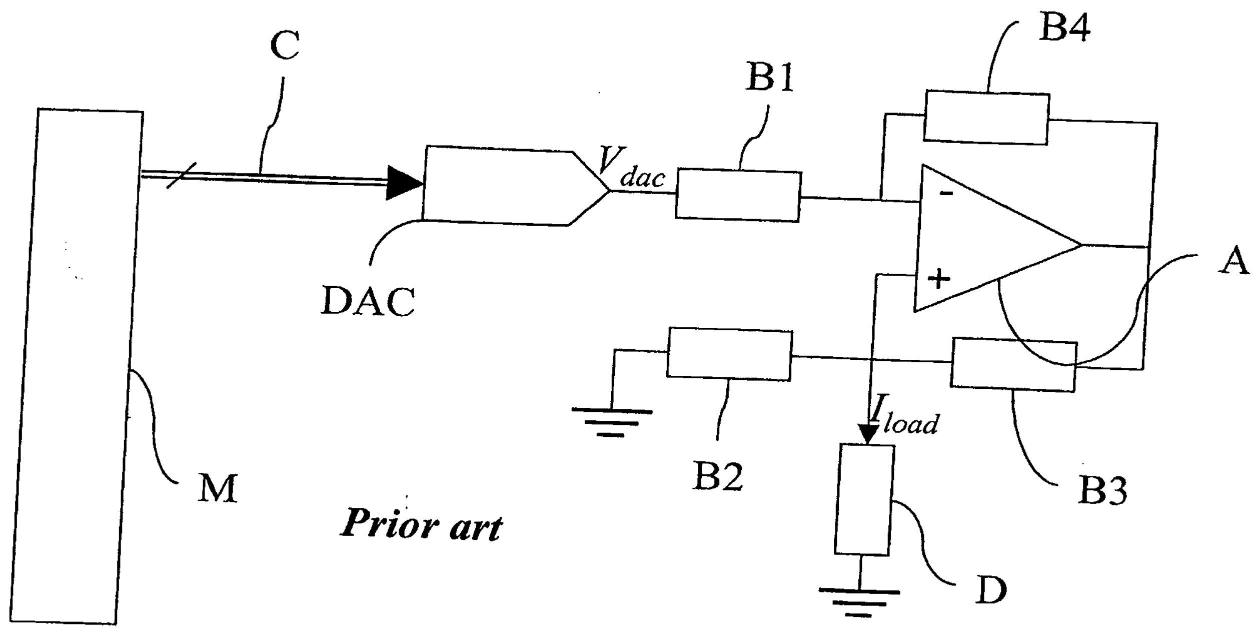
Prior art

Fig. 1



Prior art

Fig. 2



Prior art

Fig. 3

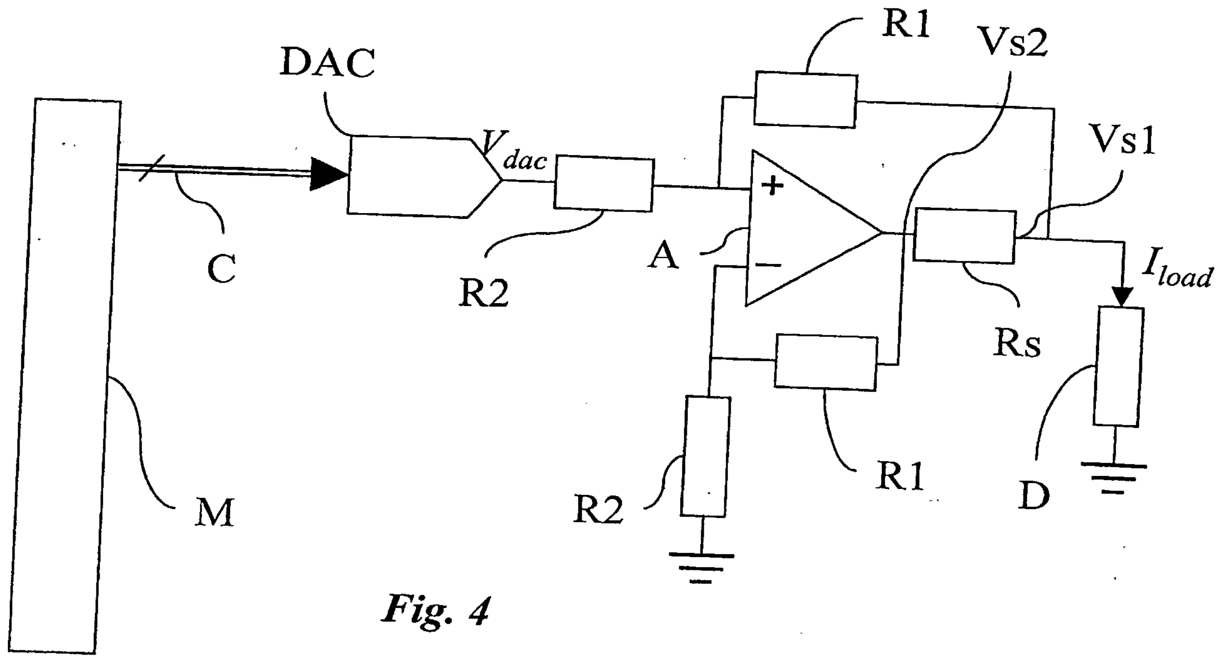


Fig. 4

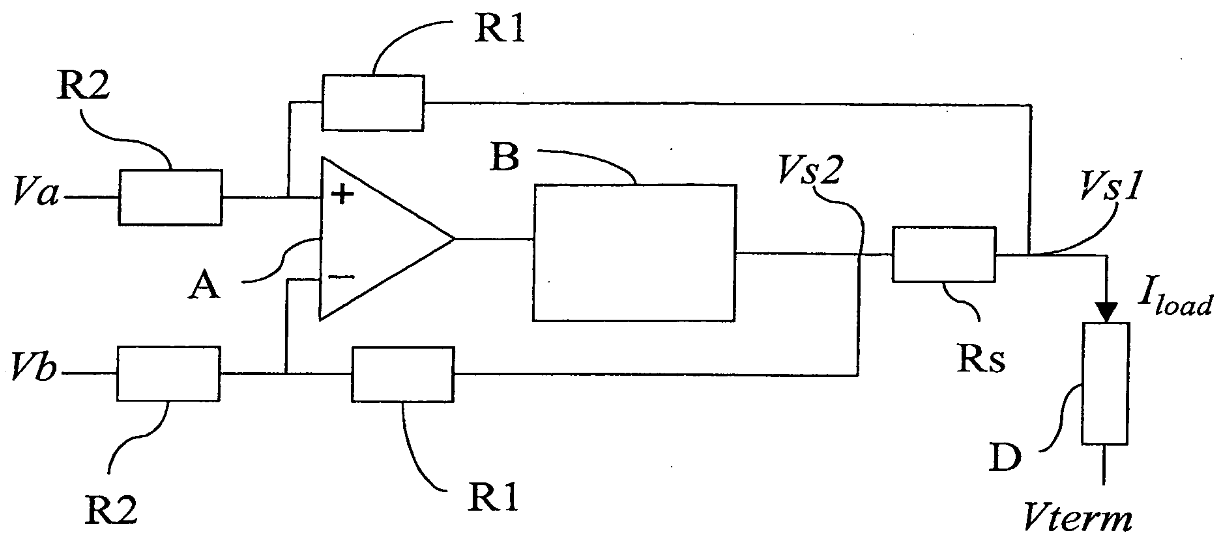

R1
R2
Va
B
Vs2
Vs1
A
I_{load}
Vb
Rs
D
R2
R1
Vterm

Fig. 5

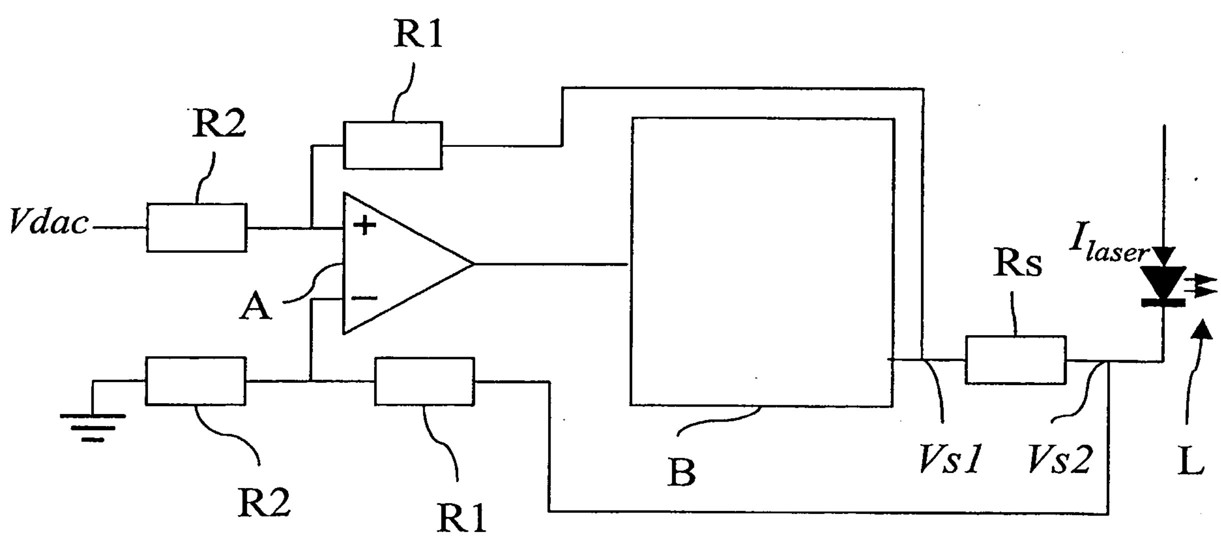

R1
R2
Vdac
A
Rs
I_{laser}
R2
R1
B
Vs1
Vs2
L

Fig. 6

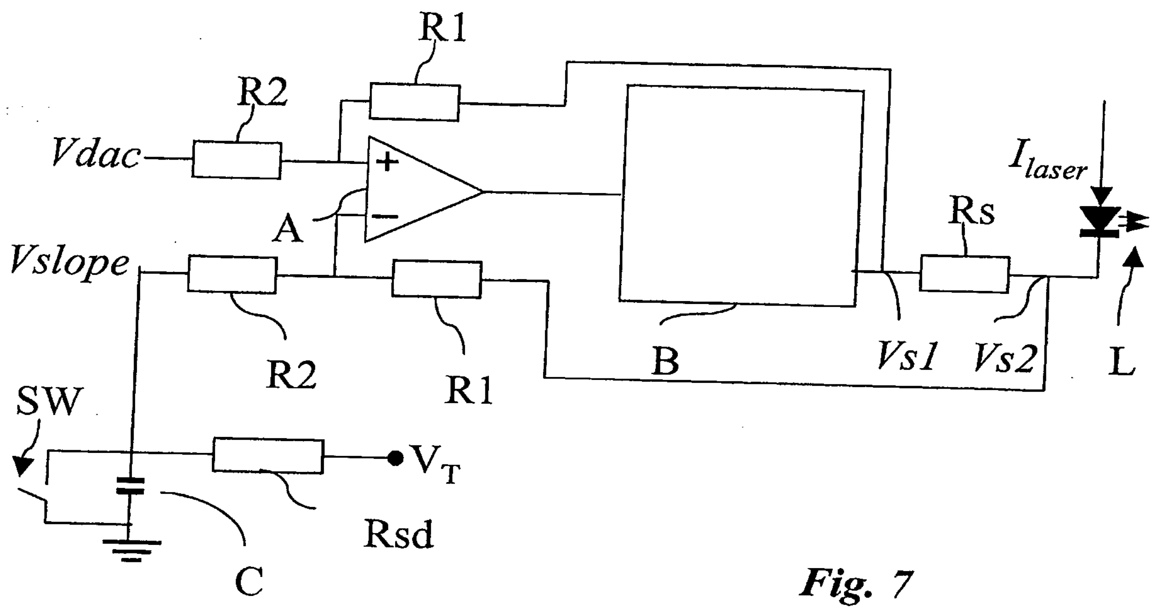


Fig. 7